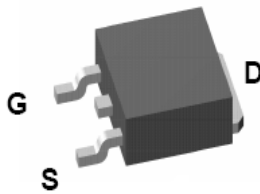


# P1003BDF

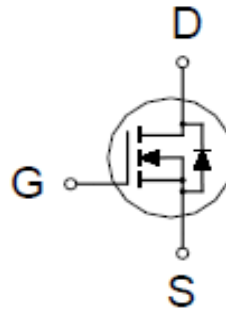
## N-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
30V	9.8m $\Omega$ @ $V_{GS} = 10V$	62A



TO-252



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>2</sup>	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	62	A
	$T_C = 100\text{ }^\circ\text{C}$		39	
Pulsed Drain Current <sup>1,2</sup>		$I_{DM}$	120	
Avalanche Current		$I_{AS}$	29	
Avalanche Energy	$L = 0.1\text{mH}$	$E_{AS}$	43	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	73	W
	$T_C = 100\text{ }^\circ\text{C}$		29	
Operating Junction & Storage Temperature Range		$T_j, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		1.7	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Package limitation current is 52A.

# P1003BDF

## N-Channel Logic Level Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.6	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>C</sub> = 70°C			10	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	120			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A		10.5	14	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		8	9.8	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 20A		55		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		1140		pF
Output Capacitance	C <sub>oss</sub>			145		
Reverse Transfer Capacitance	C <sub>rss</sub>			120		
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> = 0V, f = 1MHz		2.2		Ω
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		23		nC
Gate-Source Charge <sup>2</sup>	Q <sub>gs</sub>			5		
Gate-Drain Charge <sup>2</sup>	Q <sub>gd</sub>			6		
Turn-On Delay Time <sup>2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> ≅ 20A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 6Ω		12		nS
Rise Time <sup>2</sup>	t <sub>r</sub>			33		
Turn-Off Delay Time <sup>2</sup>	t <sub>d(off)</sub>			51		
Fall Time <sup>2</sup>	t <sub>f</sub>			25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				62	A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20A, V <sub>GS</sub> = 0V			1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20A, dI <sub>F</sub> /dt = 100A /μs		9.7		nS
Reverse Recovery Charge	Q <sub>rr</sub>				1.5	

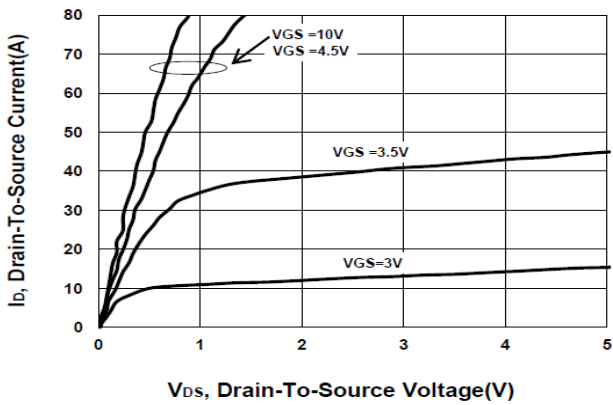
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

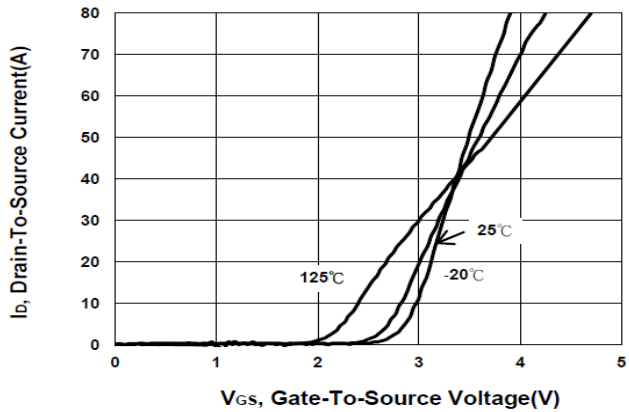
# P1003BDF

## N-Channel Logic Level Enhancement Mode MOSFET

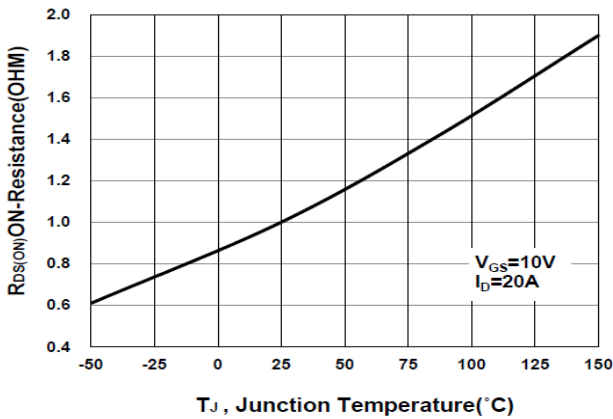
**Output Characteristics**



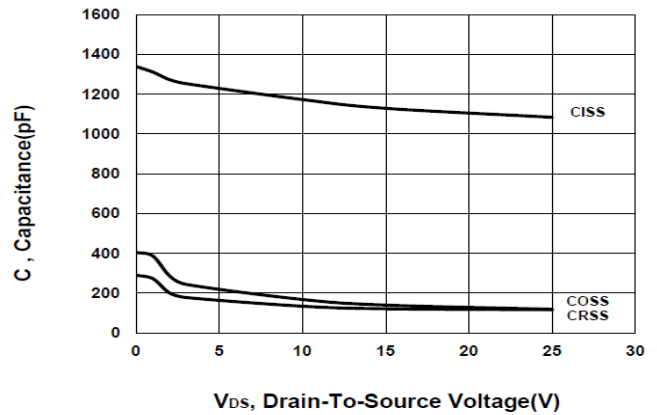
**Transfer Characteristics**



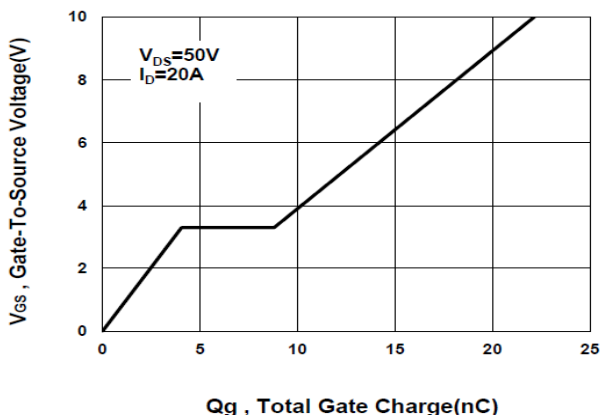
**On-Resistance VS Temperature**



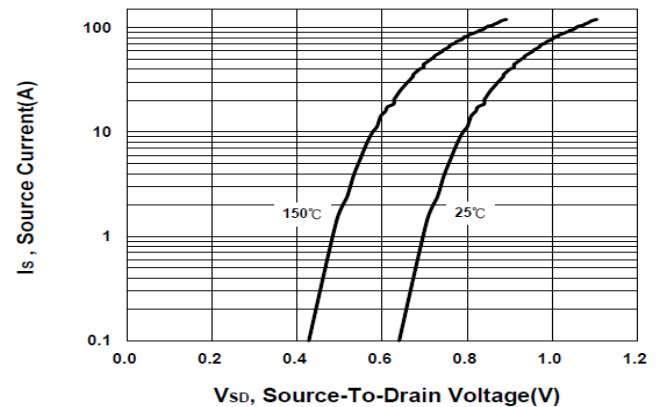
**Capacitance Characteristic**



**Gate charge Characteristics**



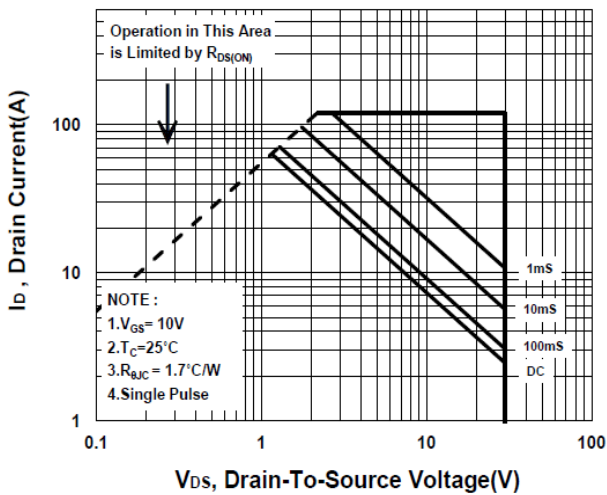
**Source-Drain Diode Forward Voltage**



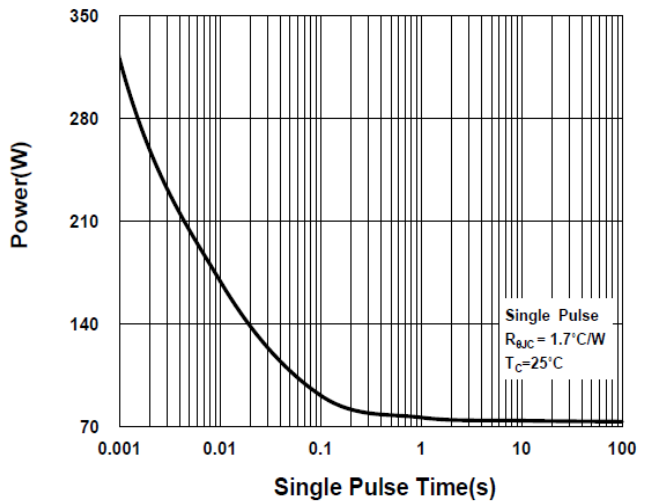
# P1003BDF

## N-Channel Logic Level Enhancement Mode MOSFET

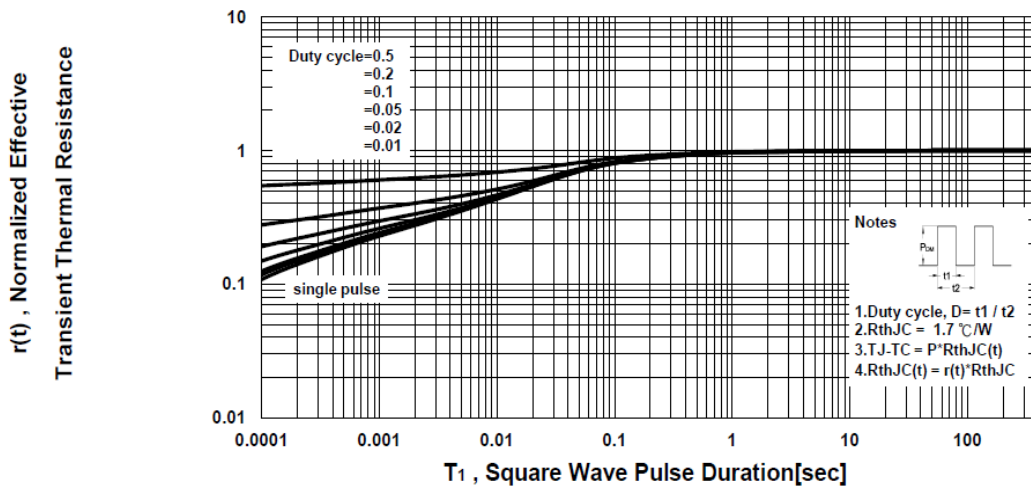
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**



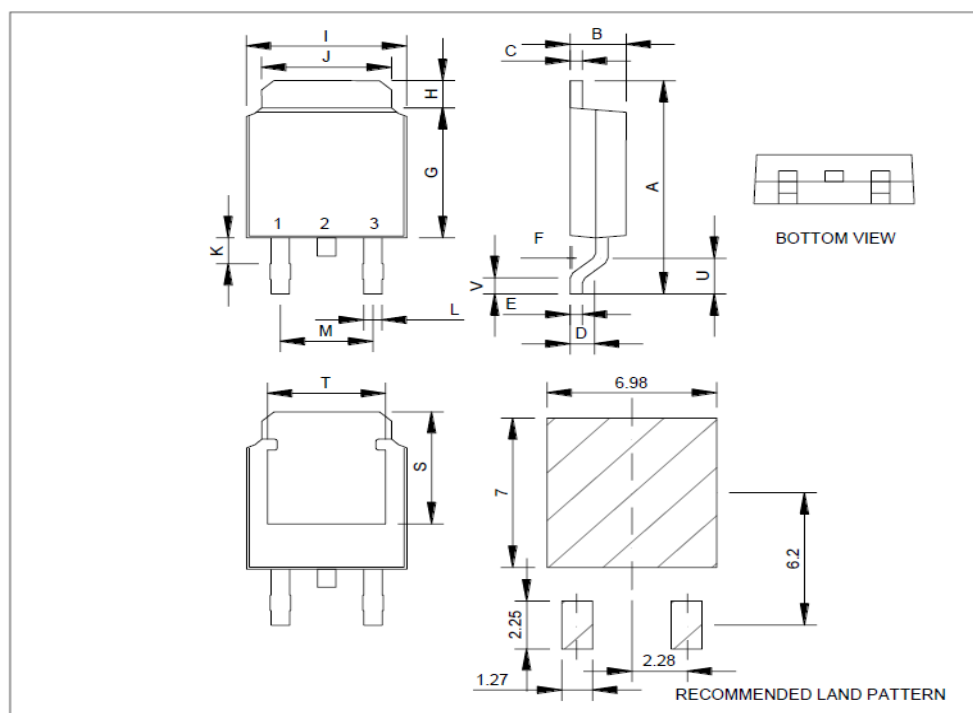
# P1003BDF

## N-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



\*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。